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(54) CMOS IC with reduced subthreshold standby leakage current

(57) The power supplies to circuit blocks in a CMOS integrated circuit, such as a very dense DRAM, are disabled during standby by series MOS switches MP1-MPm and MN1-MNm, whose substrate (back-gate) potentials VNW1-VNWm and VPW1-VPWm are changed in synchronism (figure 3) with the disabling signals applied to their gates such that standby leakage current is reduced. Some circuit blocks may have only one power switch, a direct connection being provided to the other supply.

FIG. 2

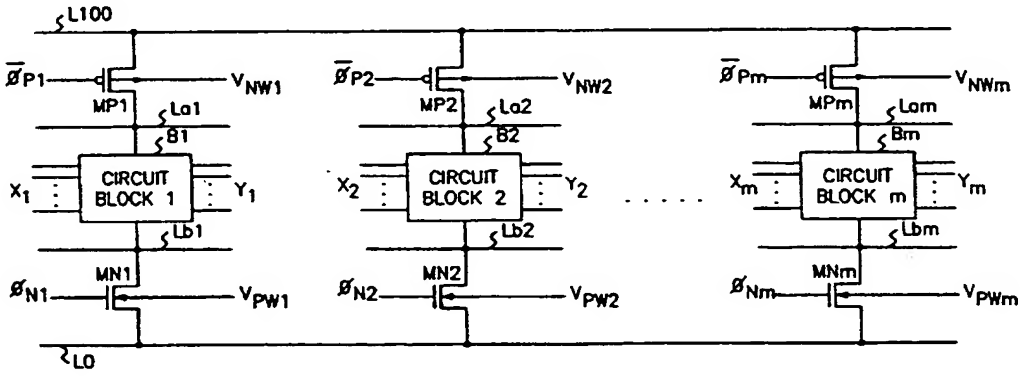

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FIG. 1

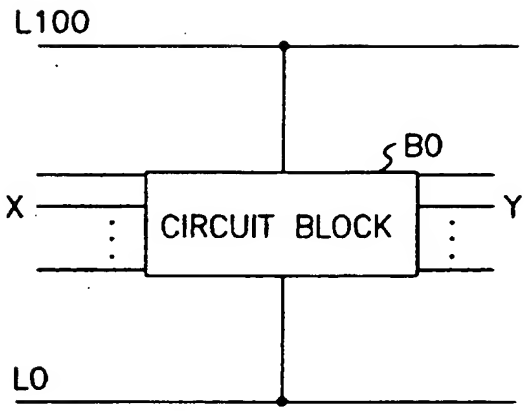


FIG. 2

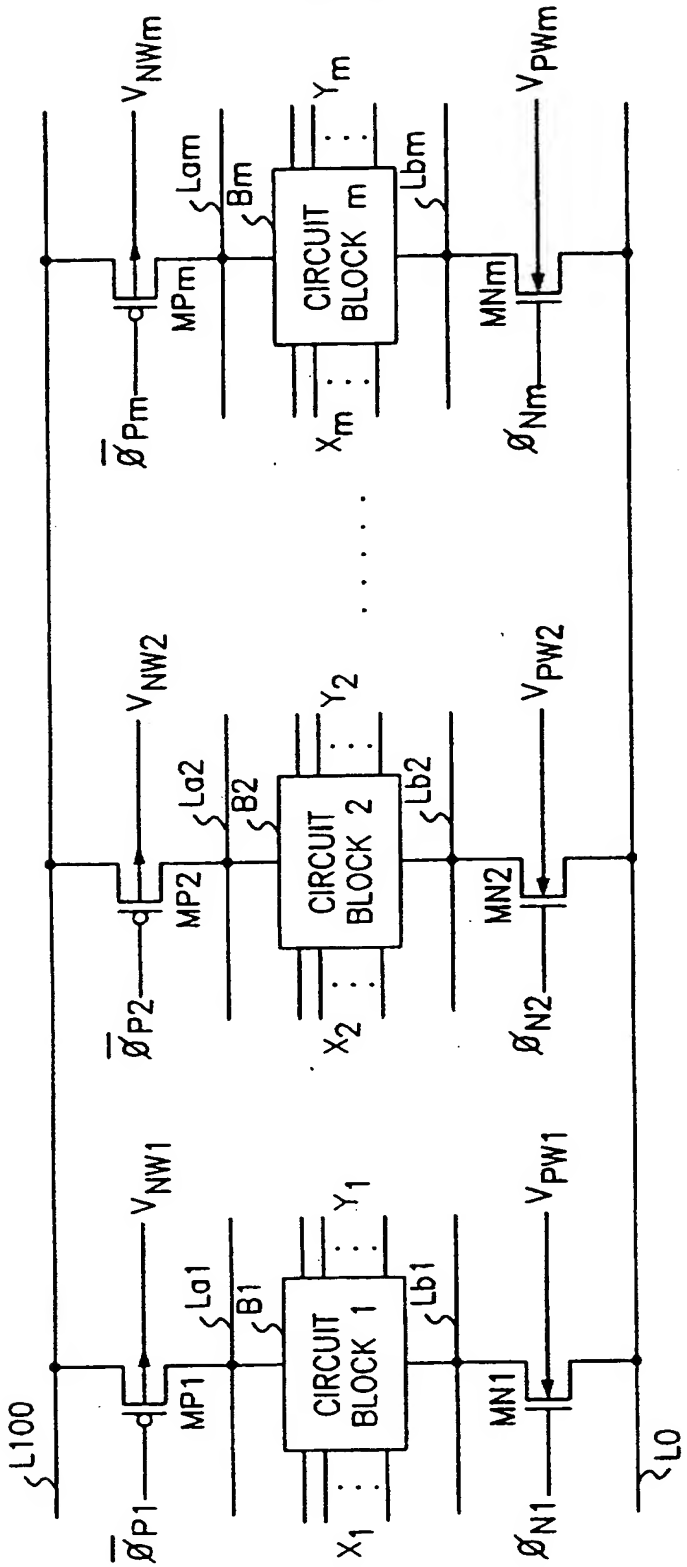

L100
L0
$\overline{\phi}_{P1}$
$\overline{\phi}_{P2}$
$\overline{\phi}_{Pm}$
ϕ_{N1}
ϕ_{N2}
ϕ_{Nm}
MP1
MP2
MPm
MN1
MN2
MNm
V_{NW1}
V_{NW2}
V_{NWm}
V_{PW1}
V_{PW2}
V_{PWm}
La1
La2
Lam
Lb1
Lb2
Lbm
B1
B2
Bm
X_1
X_2
X_m
Y_1
Y_2
Y_m
CIRCUIT BLOCK 1
CIRCUIT BLOCK 2
CIRCUIT BLOCK m

FIG. 3

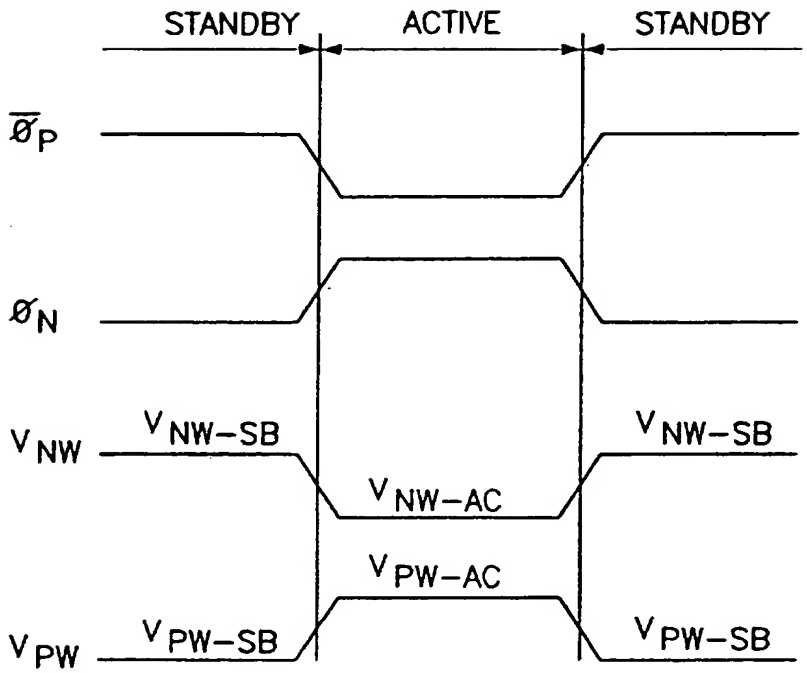

STANDBY
ACTIVE
STANDBY
$\overline{\phi}_P$
ϕ_N
V_{NW}
V_{NW-SB}
V_{NW-AC}
V_{NW-SB}
V_{PW-AC}
V_{PW}
V_{PW-SB}
V_{PW-SB}

FIG. 4

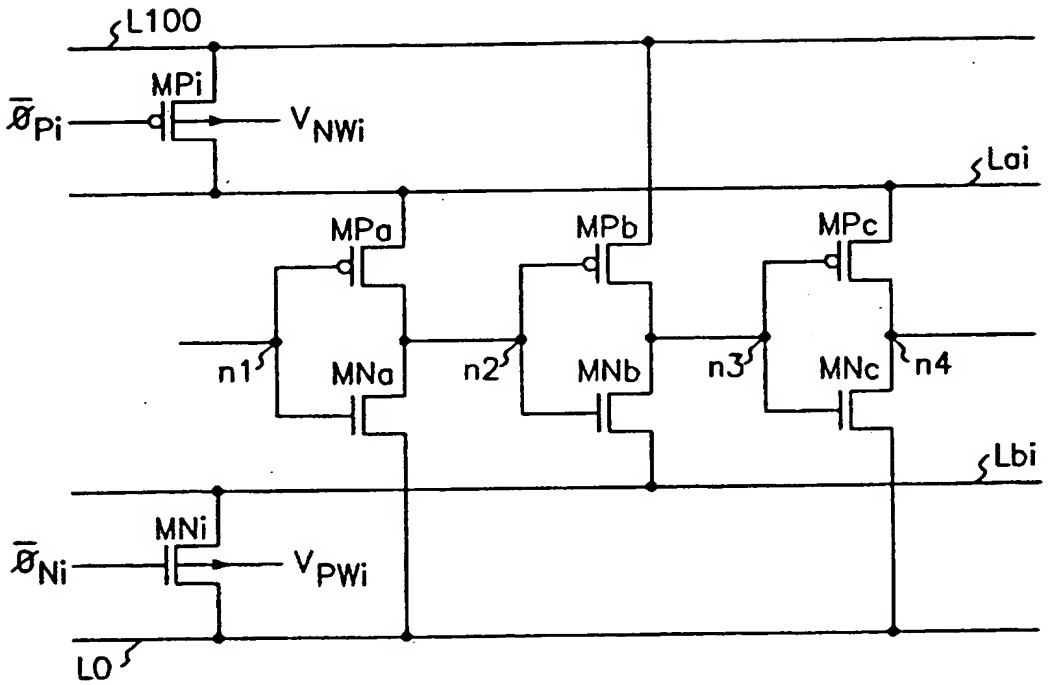

L100
MPi
$\bar{\phi}_{Pi}$
V_{NWi}
Lai
MPa
MPb
MPc
n1
MNa
n2
MNb
n3
MNc
n4
Lbi
MNi
$\bar{\phi}_{Ni}$
V_{PWi}
L0

FIG. 5A

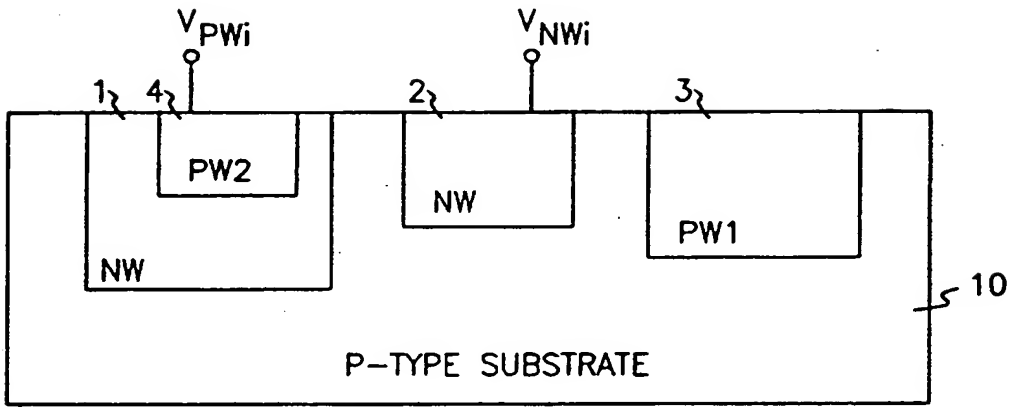
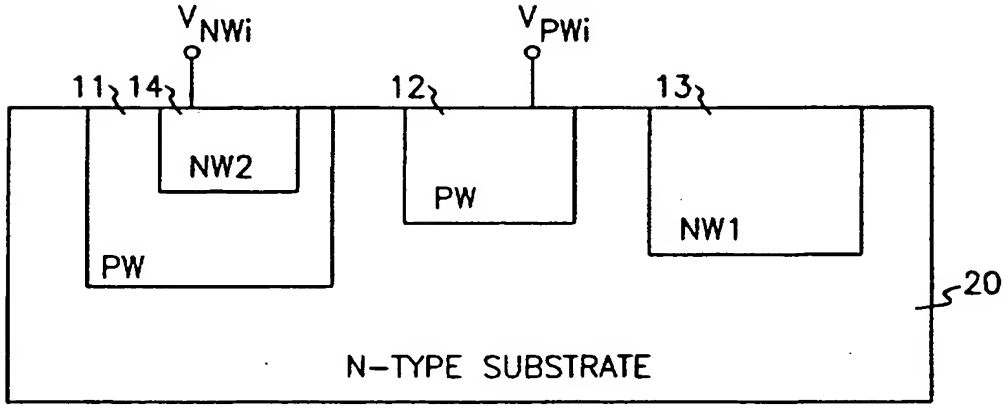

V_{PWi}
V_{NWi}
1
4
2
3
PW2
NW
PW1
NW
10
P-TYPE SUBSTRATE

FIG. 5B


V_{NWi}
V_{PWi}
11
14
12
13
NW2
PW
NW1
PW
20
N-TYPE SUBSTRATE

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SEMICONDUCTOR DEVICE FOR REDUCING POWER CONSUMPTION IN STANDBY STATE

The present invention relates to a semiconductor device for reducing power consumption due to a subthreshold current in a standby state.

In a particular arrangement to be described below and illustrative of the invention there will be described a semiconductor device suitable for being applied to a gigabit memory or logic device using a deep submicron MOS transistor having a cutoff characteristic poorer than that of a long channel transistor, to reduce dramatically a standby current, thereby decreasing power consumption in a standby state.

A previously proposed arrangement will now be described with reference to Fig. 1 of the accompanying drawings which show schematically the circuit configuration of a memory or logic device. As shown in Fig. 1, the previously proposed circuit is constructed so that a global power line L100 and global ground line L0 are directly connected to a circuit block B0. Accordingly, when the circuit uses a deep submicron MOS transistor, a lot of subthreshold current flows through the circuit, even in a cutoff state. This largely increases the power consumption in the standby state. As the MOS transistor is scaled down, its threshold voltage is decreased, resulting in an increase of the sub-

threshold current, even in a threshold region $|V_{GS}>V_T|$, of the transistor. This leads to the above problem. Therefore, in the gigabit memory device or logic device consisting of the deep submicron MOS transistors, power consumption in the standby state becomes a serious problem. To solve this problem, several techniques for the purpose of reducing power consumption in the standby state have been proposed. One of those is switched-source impedance CMOS circuit technology published in "IEEE Journal of solid state circuits, Vol. 28, 11, November 1993" by Hitachi in Japan. This technique can reduce the subthreshold current in the standby state remarkably. However, it increases the delay of the circuit. Also, the standby state to an active state transition becomes slow, decreasing the overall circuit performance.

Features of a semiconductor device to be described below, as an example, are that the transition from the standby state to the active state is fast, and the sub-threshold current in the standby state is decreased, thereby reducing its power consumption.

In a particular arrangement to be described below, as an example, there is a semiconductor device for reducing power consumption in a standby state, which has a power line providing internal circuits of the semi-conductor device with a predetermined power voltage, and

a ground line providing the internal circuits with a ground voltage, and which includes a first MOS transistor between the power line and a lower circuit block having circuits with identical timing in a standby state and in an active state respectively in the internal circuits, or between the ground line and the lower circuit block, the first MOS transistor being turned off and its threshold voltage being increased by controlling a substrate voltage when the lower circuit block is in the standby state, to reduce its subthreshold current.

Embodiments illustrative of the invention will now be described, by way of example, with reference to Figs. 2 to 5A and 5B of the accompanying drawings in which:-

Fig. 2 shows schematically the configuration of one embodiment of a semiconductor device,

Fig. 3 is a timing diagram of a control signal for use with the embodiment of Fig. 2,

Fig. 4 shows schematically the configuration of another embodiment of a semiconductor device, and

Figs. 5A and 5B are schematic diagrams showing a triple-well structure of a semiconductor device illustrative of the present invention.

Referring to the accompanying drawings, Fig. 2 shows schematically the configuration of a semiconductor device. As shown in Fig. 2, the semiconductor device is constructed in such a manner that a global power line

L100 and global ground line L0 are not directly connected to a circuit block, (B1, B2...Bm). The overall circuit blocks are divided into a plurality of lower circuit blocks, (B1, Bz...Bm), each of which consists of circuits having identical standby states and active states. Local lower power lines La1, La2...Lam, and local lower ground lines Lb1, Lb2...Lbm, corresponding to respective lower circuit blocks B1, B2...Bm are respectively connected to global power line L100 and global ground line L0 through respective switches, PMOS transistor MP1, MP2...MPm and NMOS transistor MN1, MN2...MNm thereby to form a hierarchy. An N-well and P-well on which PMOS transistor MP1 and NMOS transistor MN1 are respectively formed are separated from wells on which other MOS transistors are formed, which form a memory or logic device. Fig. 3 is a timing diagram of a control signal of Fig. 2. Since the lower circuit blocks B1, B2...Bm have identical states, the operation of one of them only will be described.

As shown in Fig. 3, a signal Φ_{Pi} inputting to the gate of PMOS transistor MP1 has a logic level "high" when lower circuit block B1 to which PMOS transistor MP1 is connected is in the standby state, and it has a logic level "low" in the case of the active state. On the other hand, a signal Φ_{Ni} inputting to the gate of NMOS transistor MN1 has a logic level "low" when lower circuit

block B1 to which NMOS transistor MN1 is connected is in the standby state, and it has a logic level "high" in the case of the active state. Accordingly, if the lower circuit block B1 is changed from the active state to the standby state, PMOS transistor MP1 and NMOS transistor MN1 are turned off according to control signal Φ_{PI}, Φ_{Ni}. As a result, lower power line La1 and lower ground line Lb1 are isolated from global power line L100 and global ground line L0, and thus power consumption in the standby state is determined by the subthreshold current which flows through PMOS transistor MP1 and NMOS transistor MN1.

As shown in Fig. 3, for the voltage V_{NWi} of the N-well on which PMOS MP1 is formed, voltage V_{NW-SB} in the standby state is higher than voltage V_{NW-AC} in the active state by a predetermined value. For the voltage V_{PWi} of the P-well on which NMOS MN1 is formed, voltage V_{PW-SB} in the standby state is lower than voltage V_{PW-AC} in the active state by a predetermined value. As a result, respective threshold voltages of PMOS transistor MP1 and NMOS transistor MN1 are increased according to body effect. Accordingly, the subthreshold currents of PMOS transistor MP1 and NMOS transistor MP1 in the standby state are remarkably decreased, resulting in a reduction of the power consumption.

Meanwhile, if the standby state is changed to the

active state, control signal Φ_{Pi} is changed from a logic level "high" to a logic level "low", and control signal Φ_{Ni} from a logic level "low" to a logic level "high". At the same time voltage V_{NWi} is decreased from voltage V_{NW-SB} to voltage V_{NW-AC}, and in turn voltage V_{PWi} is increased from voltage V_{PW-SB} to voltage V_{PW-AC}, thereby reducing the respective threshold voltages of PMOS transistor MP1 and NMOS transistor MN1. Accordingly, the standby state to active state transition occurs quickly. That is, the respective well voltages of PMOS transistor MP1 and NMOS transistor MN1 are different from each other in the standby state and the active state. As a result, the threshold voltage is increased in the standby state, reducing the threshold current. On the other hand, the threshold voltage is decreased in the active state so that the standby state to the active state transition occurs quickly, and at the same time, the current driving capabilities of PMOS transistor MP1 are NMOS transistor MN1 are improved. Referring to Fig. 2, one of global power line L100 and global ground line L0 may be directly connected to the circuit block, and the other one may be used for hierarchy using the lower power line.

Generally, in a memory device such as a dynamic random access memory (DRAM), the logic level of an internal node is fixed in the standby state. In this case, the subthreshold current can be more effectively

reduced. Fig. 4 shows a method for connecting a power line to an internal circuit having a fixed logic level in the standby state. The circuit block shown in Fig. 4 consists of three serially connected inverters. In this circuit, if an input node n1 of the inverter is logic "high", node n2 logic "low", node n3 logic "high", and node n4 logic "low", the subthreshold current of PMOS transistor MPa, NMOS transistor MNb, and PMOS transistor MPc cause lower power line Lai to decrease its voltage, and lower ground line Lbi to increase its voltage. Here, as shown in Fig. 4, transistors MPa, MNb and MPc as paths of the subthreshold current, are connected to lower power line Lai or lower ground line Lbi, and other transistors are connected to global power line L100 and global ground line L0, and a reverse voltage is applied between the gates and the sources of transistors MPa, MNb and MPc. This reduces the subthreshold current considerably. Similarly, the subthreshold current of the MOS transistor is abruptly decreased if the reverse voltage is applied between its gate and source.

The voltage of lower power line Lai is decreased by some quantity of value ΔV_{DD} in comparison with the voltage of global power line L100, due to the subthreshold current. On the other hand, the voltage of lower ground line Lbi is increased by some quantity of value ΔV_{SS} in comparison with the voltage of global ground line L0, due

to the subthreshold current. Accordingly, the reverse bias corresponding to the voltage difference ΔV_{DD} is applied between the gates and sources of transistors MPa and MPc, and the reverse bias corresponding to voltage the difference ΔV_{SS} is applied between the gate and source of the transistor MNb.

Figs. 5A and 5B are schematic diagrams showing a triple-well structure for the purpose of realizing a semiconductor device illustrative of the arrangement of Fig. 4. Since the substrate voltages of PMOS transistor MPi and NMOS transistor MNi, which serve as switches between the global power line and global ground line, and the lower power line and lower ground line, should be isolated from the substrate voltages of the other transistors forming the internal circuits, the transistors MPi and MNi should be formed on wells separated from each other. That is, the triple-well structure is suitable for forming PMOS transistor MPi and NMOS transistors MNi on separate wells in order to contro freely the voltage of the well (substrate voltage).

Fig. 5A shows a triple-well consisting of a first N-well 1 and second N-well 2 which are separated from each other and formed on a P-type substrate 10, a first P-well 3 separated from first and second N-wells 1 and 2, and a second P-well 4 formed in first N-well 1. PMOS transistor MPi serving as a switch between the global

power line and the lower power line is formed in second N-well 2, and NMOS transistor MNi serving as a switch between the global ground line and the lower ground line is formed in second P-well 4. Accordingly, even if the well voltages, V_{NWi} and V_{PWi} are changed, other transistors forming the circuit are not affected. Fig. 5B shows a triple-well structure according to the other embodiment of the present invention. This triple-well consists of a first P-well 11 and second P-well 12 which are separated from each other and formed on an N-type substrate 20, a first N-well 13 separated from first and second P-wells 11 and 12, and a second N-well 14 formed in the first P-well 11. PMOS transistor MPi serving as a switch between the global power line and the lower power line is formed in second N-well 14, and NMOS transistor MNi serving as a switch between the global ground line and the lower ground line is formed in the second P-well 12. Accordingly, even if the well voltages V_{NWi} and V_{PWi} are changed, other transistors forming the circuit are not affected.

In the case that one of the global power line L100 and the global ground line L0 is directly connected to the circuit block, and the other one is used for hierarchy using the lower power line, only one of second P-well 4 and second N-well 2 may be formed on which the switching transistors are formed, as shown in Fig. 5A.

Also, in the case of the device shown in Fig. 5B, the well may be formed according to the same principle as that of the aforementioned case.

As described, in the above embodiments of the present invention, the standby state to the active state transition becomes fast, and power consumption is reduced by decreasing the subthreshold current in the standby state, thereby improving the reliability of a high integration memory or logic device used for portable electronic products requiring low power consumption.

It will be understood that, although the present invention has been illustrated, by way of example, with reference to particular embodiments, variations and modifications thereof, as well as other embodiments, may be made within the scope of the protection sought by the appended claims.

CLAIMS

1. A semiconductor device for reducing power consumption in a standby state, having a power line providing internal circuits of the semiconductor device with a predetermined power voltage, and a ground line providing the internal circuits with a ground voltage, the semiconductor device including a first MOS transistor provided between the power line and a lower circuit block which includes circuits having identical timing in a standby state and an active state in the internal circuits, or between the ground line and the lower circuit block, the first MOS transistor being turned off and its threshold voltage being increased by controlling a substrate voltage when the lower circuit block is in the standby state, to reduce its subthreshold current.

2. A semiconductor device for reducing power consumption in a standby state as claimed in claim 1, wherein in the case in which predetermined nodes of the lower circuit block have a fixed logic level in the standby state, a second MOS transistor, providing a path for subthreshold current of second MOS transistors forming the lower circuit block, is connected to the power line or the ground line through the first MOS transistor and the other second MOS transistor which is not to provide a path for the subthreshold current is

directly connected to the power line or the ground line.

3. A semiconductor device for reducing power consumption in a standby state as claimed in claim 1, wherein the gate of the first MOS transistor between the power line and the lower circuit block receives a logic level "high" when the lower circuit block to which the first MOS transistor connected is in the standby state, and receives a logic level "low" when the lower circuit block to which the first MOS transistor connected is in the active state, the first MOS transistor being a P-channel MOS transistor having a substrate voltage, and the substrate voltage in the active state being lower than that in the standby state by a predetermined value.

4. A semiconductor device for reducing power consumption in a standby state as claimed in claim 1, wherein the gate of the first MOS transistor between the ground line and the lower circuit block receives a logic level "low" when the lower circuit block to which the first MOS transistor connected is in the standby state, and receives a logic level "high" when the lower circuit block to which the first MOS transistor connected is in the active state, the first MOS transistor being a N-channel MOS transistor having a substrate voltage, and the substrate voltage in the active state being higher than that in the standby state by a predetermined value.

5. A semiconductor device for reducing power

consumption in a standby state as claimed in claim 4, wherein the first MOS transistor is on a separate well to control freely the substrate voltage without affecting the second MOS transistor of the lower circuit block.

6. A semiconductor device as claimed in claim 1 including an arrangement substantially as described herein with reference to Fig. 2, Fig. 4 or Fig. 5 of the accompanying drawings.

7. A method of operating a semiconductor device as claimed in claim 1 substantially as described herein with reference to Fig. 3 of the accompanying drawings.